

Appn. #09/651,422

REMARKS

Claim 12 is cancelled; claims 9 and 13 are amended; new claims 32 and 33 are added; claims 9, 10, 13, 32 and 33 are pending in the application.

Claims 9, 10 and 13 stand rejected as being unpatentable over Wu (U.S. Patent No. 5,915,182); Wu (U.S. Patent No. 6,107,149); Ju et al. (U.S. Patent No. 6,232,166) and Tsukamoto et al. (U.S. Patent No. 5,700,349), in various combinations. Applicant has amended claim 9, from which claims 10 and 13 depend, and believes that such amendment places claims 9, 10 and 13 in condition for allowance.

Amended claim 9 recites a method of forming a transistor structure in which an electrically insulative material is formed along a transistor gate sidewall and such is subsequently anisotropically etched to form a spacer along the transistor gate sidewall. The claim further recites that the electrically insulative material comprises a first layer comprising Al_pO_q and a second layer consisting essentially of silicon and nitrogen, with the first layer being between the second layer and the transistor gate sidewall. Additionally, the claim recites that both of the first and second layers are anisotropically etched by the etching process.

Amended claim 9 is believed allowable over the cited references for at least the reason that the references do not suggest or disclose the claim 9 recited feature of two layers anisotropically etched to form a sidewall spacer, with the layer closest to the sidewall comprising Al_pO_q , and the other layer consisting essentially of silicon and nitrogen.

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The only cited reference which discloses a sidewall comprising Al_pO_q is Tsukamoto. However, such reference does not suggest or disclose that the Al_pO_q is between a transistor gate sidewall and another layer consisting essentially of silicon and nitrogen. The Examiner's other cited references indicate that silicon oxynitride can be formed between a sidewall of a transistor gate and silicon nitride, but, like Tsukamoto, contain no disclosure that Al_pO_q can be formed between a sidewall of the transistor gate and a layer consisting essentially of silicon and nitrogen.

The Examiner contends that Tsukamoto teaches that silicon oxynitride and aluminum oxide are functional equivalents, and accordingly, it would be obvious to substitute aluminum oxide for the silicon oxynitride of the Wu and Ju references. Applicant respectfully submits that regardless of any teaching within Tsukamoto that aluminum oxide can be substituted for silicon oxynitride in the specifically-described structures; such does not render it obvious to substitute aluminum oxide for silicon oxynitride in the structures of Wu and Ju. Applicant further submits that the claim 9 recited structure having aluminum oxide between a gate sidewall and a layer consisting of silicon and nitrogen can, in particular aspects, protect the Al_pO_q from dopant diffusion (see, for example, page 6, lines 12-16 of the originally filed application). The Examiner's cited references do not suggest this, or any other motivation, for substituting Al_pO_q for the silicon oxynitride materials of the Wu and Ju references. Claim 9 is therefore believed allowable over the cited references, and Applicant requests such allowance in Examiner's next action.

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Claims 10 and 13 depend from claim 9, therefore and are allowable for at least the reasons discussed above regarding claim 9.

New claims 32 and 33 also depend from claim 9, and are therefore believed allowable for at least the reasons discussed above regarding claim 9. New claims 32 and 33 are supported by the originally filed application at, for example, page 9, lines 8-19 and therefore do not comprise "new matter".

Pending claims 9, 10, 13, 32 and 33 are allowable for the reasons discussed above, and Applicant therefore requests formal allowance of such claims in the Examiner's next action.

Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No.09/651,422
Filing DateAugust 30, 2000
Inventor..... Jeffrey W. Honeycutt et al.
Assignee.....Micron Technology, Inc.
Group Art Unit.....2815
Examiner A. Wilson
Attorney's Docket No.MI22-1332
Title: Methods of Forming Insulative Material Against Conductive Structures

VERSION WITH MARKINGS TO SHOW CHANGES MADE
ACCOMPANYING RESPONSE TO OFFICE ACTION MAILED NOVEMBER 21, 2002

In the Claims

Cancel claims 12 and 13. ^{N.E}

9. (Amended) A method of forming a transistor structure, comprising:
- forming a transistor gate over a substrate, the transistor gate comprising a sidewall which comprises electrically conductive material;
- forming an electrically insulative material along the electrically conductive material of the transistor gate sidewall; the electrically insulative material comprising at least two separate layers; ~~the at least two layers having different chemical compositions from one another;~~ a first of the at least two layers comprising ~~at least one of Si₃O₄N₂ or Al₂O₃.~~

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wherein p , q , ~~x , y and z~~ are greater than 0 and less than 10; a second of the at least two layers consisting essentially of silicon and nitrogen; and

anisotropically etching the electrically insulative material to form a spacer along the transistor gate sidewall; the anisotropically etching comprising etching both of the first and second of the at least two layers; and

wherein the first of the at least two layers is between the second of the at least two layers and the transistor gate sidewall.

13. (Amended) The method of claim 9 wherein the first of the at least two layers consists essentially of the Al_pO_q and ~~is between the second of the at least two layers and the transistor gate sidewall.~~

32. (New) The method of claim 9 wherein the first of the at least two layers consists of Al_pO_q .

33. (New) The method of claim 9 wherein the first of the at least two layers consists of Al_2O_3 .

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